

What is claimed is:

1           1.       A method for forming a semiconductor device, comprising:  
2               forming a first pattern for a semiconductor device in a semiconductor  
3       device formation region of a semiconductor substrate and simultaneously  
4       forming the first pattern in a first mark formation region of the semiconductor  
5       substrate;  
6               forming a second pattern for the semiconductor device on a resultant  
7       structure in the semiconductor device formation region of the semiconductor  
8       substrate and simultaneously forming the second pattern in a second mark  
9       formation region of the semiconductor substrate; and  
10              inspecting the first pattern in the first mark formation region and the  
11              second pattern in the second mark formation region for misalignments.

1           2.       The method for forming a semiconductor device as claimed in  
2       claim 1, wherein the first mark formation region is a box shaped main scale  
3       formation region, and the second mark formation region is a box shaped  
4       vernier formation region.

1           3.       The method for forming a semiconductor device as claimed in  
2       claim 2, wherein the first pattern is an active pattern in a DRAM cell region,  
3       and the second pattern is a word line pattern in the DRAM cell region.

1           4.       The method for forming a semiconductor device as claimed in  
2       claim 1, wherein a scattering bar is formed at an edge of a pattern in a mask  
3       corresponding to the first pattern in the first mark formation region.

1           5.       The method for forming a semiconductor device as claimed in  
2       claim 1, wherein a scattering bar is formed at an edge of a pattern in a mask  
3       corresponding to the second pattern in the second mark formation region.

1           6.       A semiconductor device having an overlay mark, the overlay  
2       mark, comprising:

3           a first mark formed in a first mark formation region of a semiconductor  
4       substrate and a first pattern formed in a semiconductor device formation region  
5       of the semiconductor substrate, wherein the first mark and the first pattern are  
6       formed simultaneously by a same process such that the first mark has a shape  
7       identical to a shape of the first pattern; and

8           a second mark formed in a second mark formation region of the  
9       semiconductor substrate and a second pattern formed in the semiconductor  
10      device formation region of the semiconductor substrate, wherein the second  
11      mark and the second pattern are formed simultaneously by a same process  
12      such that the second mark has a shape identical to a shape of the second  
13      pattern.

1           7.       The semiconductor device as claimed in claim 6, wherein the  
2       first mark formation region is a box shaped main scale formation region, and  
3       the second mark formation region is a box shaped vernier formation region.

1           8.       The semiconductor device as claimed in claim 7, wherein the  
2       first pattern is an active pattern in a DRAM cell region, and the second pattern  
3       is a word line pattern in the DRAM cell region.